What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A capacitor for a semiconductor device, said capacitor comprising:

a bottom conducting layer;

a dielectric layer deposited on said bottom conducting layer; and

an oxygen permeable top conducting layer deposited and annealed on said dielectric layer.

2. The capacitor of claim 1, wherein said bottom conducting layer is formed of a material selected from the noble metal group.

3. The capacitor of claim 1, wherein said bottom conducting layer is formed of a metal.

4. The capacitor of claim 1, wherein said bottom conducting layer is formed of a metal alloy.

5. The capacitor of claim 1, wherein said bottom conducting layer is formed of a conducting metal oxide.

6. The capacitor of claim 1, wherein said bottom conducting layer is formed of a metal nitride.

7. The capacitor of claim 1, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuQ_2), Rhodium Oxide (RhO_2), Chromium Oxide (CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO_2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides

(VO_1 or VO_2), Niobium Oxides (NbO_1 or NbO_2), and Tungsten Nitride (WNx, WN, or W_2N).

8. The capacitor of claim 7, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), and Tungsten Nitride (WNx, WN, or W_2N).

9. The capacitor of claim 1, wherein said bottom conducting layer is placed on top of an oxygen barrier.

10. The capacitor of claim 1, wherein said dielectric layer is a dielectric metal oxide layer.

11. The capacitor of claim 1, wherein said dielectric layer has a dielectric constant between 7 and 300.

12. The capacitor of claim 1, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Aluminum Oxide (Al_2O_3), Zirconium Oxide (ZrO_2), Praseodymium Oxide (PrO_2), Tungsten Oxide (WO_3), Niobium Pentoxide (Nb_2O_5), Strontium Bismuth Tantalate (BST), Hafnium Oxide (HfO_2), Hafnium Silicate, Lanthanum Oxide (La_2O_3), Yttrium Oxide (Y_2O_3) and Zirconium Silicate.

13. The capacitor of claim 12, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Strontium Bismuth Tantalate (SBT), Aluminum Oxide (Al_2O_3), Zirconium Oxide (ZrO_2) and Hafnium Oxide (HfO_2).

14. The capacitor of claim 13, wherein said dielectric layer is Tantalum Oxide and is amorphous or crystalline.

15. The capacitor of claim 1, wherein said top conducting layer is formed of a material selected from the noble metal group.

16. The capacitor of claim 1, wherein said top conducting layer is formed of a non-oxidizing metal permeable to oxygen.

17. The capacitor of claim 1, wherein said top conducting layer is formed of a conducting metal oxide.

18. The capacitor of claim 1, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2), Chromium Oxide (CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO_2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), and Niobium Oxides (NbO_1 or NbO_2).

19. The capacitor of claim 18, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), and Platinum Iridium (PtIr).

20. The capacitor of claim 1, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said dielectric layer is a layer of Tantalum Oxide.

21. The capacitor of claim 1, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said dielectric layer is a layer of Barium Strontium Titanate (BST).

22. The capacitor of claim 1, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said bottom conducting layer is a layer of Tungsten Nitride (WNx, WN, or W_2N) layer and said dielectric layer is a layer of Aluminum Oxide (Al_2O_3).

23. The capacitor of claim 1, wherein said top conducting layer is annealed with an oxygen compound.

24. The capacitor of claim 23, wherein said oxygen annealed layer is one annealed in the presence of a material selected from the group consisting of: Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O).

25. The capacitor of claim 23, wherein said oxygen annealed layer is one annealed in the presence of a gas mixture containing at least one element selected from the group consisting: Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O).

26. The capacitor of claim 23, wherein oxygen annealed layer is a plasma enhanced annealed layer.

27. The capacitor of claim 26, wherein said oxygen containing anneal is a remote plasma enhanced anneal.

28. The capacitor of claim 23, wherein said oxygen containing anneal is an ultraviolet light enhanced anneal.

29. The capacitor of claim 1, wherein said capacitor is a stacked capacitor.

30. The capacitor of claim 1, wherein further comprising an access transistor connected to said capacitor.

31. The capacitor of claim 1, wherein said capacitor forms part of a dynamic random access memory cell.

32. A method of forming a capacitor in a semiconductor device, said method comprising:

forming a bottom conducting layer;

forming a dielectric layer over the bottom conducting layer;

forming a top conducting layer over the dielectric layer; and

annealing the top conducting layer after it is formed.

33. A method of forming a capacitor of claim 32, wherein said capacitor is formed over a conductive plug, said method further comprising depositing an oxygen barrier over said conductive plug prior to forming the bottom conducting layer.

34. A method of forming a capacitor of claim 32, said method further comprising:

annealing the dielectric layer after it is formed.

35. A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a material selected from the noble metal group.

36. A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a metal.

37. A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a metal alloy.

38. A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a conducting metal oxide.

39. A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a metal nitride.

40. A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2), Chromium Oxide (CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO_2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), Niobium Oxides (NbO_1 or NbO_2), and Tungsten Nitride (WNx, WN or W_2N).

41. A method of forming a capacitor of claim 40, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), and Tungsten Nitride (WNx, WN or W_2N).

42. A method of forming a capacitor of claim 32, wherein said dielectric layer is a dielectric metal oxide layer.

43. A method of forming a capacitor of claim 32, wherein said dielectric layer has a dielectric constant between 7 and 300.

44. A method of forming a capacitor of claim 32, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Aluminum Oxide (Al_2O_3), Zirconium Oxide (ZrO_2), Praseodymium Oxide (PrO_2), Tungsten Oxide (WO_3), Niobium Pentoxide (Nb_2O_5), Strontium Bismuth Tantalate (SBT), Hafnium Oxide (HfO_2), Hafnium Silicate, Lanthanum Oxide (La_2O_3), Yttrium Oxide (Y_2O_3), and Zirconium Silicate.

45. A method of forming a capacitor of claim 44, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Strontium Bismuth Tantalate (BST), Aluminum Oxide (Al_2O_3), Zirconium Oxide (ZrO_2) and Hafnium Oxide (HfO_2).

46. A method of forming a capacitor of claim 45, wherein said dielectric layer is Tantalum Oxide and is crystalline or amorphous material.

47. A method of forming a capacitor of claim 46, wherein said amorphous dielectric layer is heated to a temperature above 200 degrees Celsius to change said dielectric layer from an amorphous material to a crystalline material.

48. A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a material selected from the noble metal group.

49. A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a non-oxidizing metal permeable to oxygen.

50. A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a conducting metal oxide.

51. A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2), Chromium Oxide (CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO_2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), and Niobium Oxides (NbO_1 or NbO_2).

52. A method of forming a capacitor of claim 51, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), and Platinum Iridium (PtIr).

53. A method of forming a capacitor of claim 32, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: Platinum,

Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said dielectric layer is a layer of Tantalum Oxide.

54. A method of forming a capacitor of claim 32, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said dielectric layer is a layer of Barium Strontium Titanate (BST) or Strontium Bismuth Tantalate (SBT).

55. A method of forming a capacitor of claim 32, wherein said top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said bottom conducting layer is a layer of Tungsten Nitride (WNx, WN or W_2N) layer and said dielectric layer is a layer of Aluminum Oxide (Al_2O_3).

56. A method of forming a capacitor of claim 32, wherein said annealing is performed with an oxidizing gas.

57. A method of forming a capacitor of claim 56, wherein said annealing is performed with a material selected from the group consisting of: Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O).

58. A method of forming a capacitor of claim 57, wherein said annealing is performed with a gas mixture containing at least one element selected from the group consisting: Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O).

59. A method of forming a capacitor of claim 56, wherein said annealing is a plasma enhanced annealing.

60. A method of forming a capacitor of claim 59, wherein said annealing is a remote plasma enhanced annealing.

61. A method of forming a capacitor of claim 56, wherein said annealing is an ultraviolet light enhanced annealing.

62. A method of forming a capacitor of claim 32, wherein said annealing is performed at a temperature between 300 and 800 degrees Celsius.

63. A method of forming a capacitor of claim 62, wherein said annealing is performed at a temperature between 400 and 750 degrees Celsius.

64. A method of forming a capacitor of claim 32, wherein said annealing is performed at a pressure between 1 and 760 torr.

65. A method of forming a capacitor of claim 64, wherein said annealing is performed at a pressure between 2 and 660 torr.

66. A method of forming a capacitor of claim 32, wherein said annealing is performed for between 10 seconds and 60 minutes.

67. A method of forming a capacitor of claim 66, wherein said annealing is performed for between 10 seconds and 30 minutes.

68. A method of forming a capacitor of claim 32, wherein said annealing is performed in the presence of an oxygen as with a gas flow rate between 0.01 and 10 liters per second.

69. A processor system comprising:

a processor;

and a memory device coupled to said processor further comprising a capacitor structure, wherein said capacitor structure comprises:

a bottom conducting layer;

a dielectric layer deposited on said bottom conducing layer; and

an oxygen permeable top conducting layer deposited and annealed on said dielectric layer.

70. A processor system of claim 69, wherein said capacitor further comprises:

an annealed dielectric layer after it is formed.

71. The system of claim 69, wherein said bottom conducting layer is formed of a material selected from the noble metal group.

72. The system of claim 69, wherein said bottom conducting layer is formed of a metal.

73. The system of claim 69, wherein said bottom conducting layer is formed of a metal alloy.

74. The system of claim 69, wherein said bottom conducting layer is formed of a conducting metal oxide.

75. The system of claim 69, wherein said bottom conducting layer is formed of a metal nitride.

76. The system of claim 69, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2), Chromium Oxide (CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide (ReO_3), Iridium Oxide (IrO_2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), Niobium Oxides (NbO_1 or NbO_2), and Tungsten Nitride (WN, WNX, or W_2N).

77. The system of claim 76, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), and Platinum Iridium (PtIr), and Tungsten Nitride (WN, WNX, or W_2N).

78. The system of claim 69, wherein said bottom conducting layer is placed on top of an oxygen barrier.

79. The system of claim 69, wherein said dielectric layer is a dielectric metal oxide layer.

80. The system of claim 69, wherein said dielectric layer has a dielectric constant between 7 and 300.

81. The system of claim 69, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Aluminum Oxide (Al_2O_3), Zirconium Oxide (ZrO_2), Praseodymium Oxide (PrO_2), Tungsten Oxide (WO_3), Niobium Pentoxide (Nb_2O_5), Strontium Bismuth Tantalate (SBT), Hafnium Oxide (HfO_2), Hafnium Silicate, Lanthanum Oxide (La_2O_3), Yttrium Oxide (Y_2O_3) and Zirconium Silicate.

82. The system of claim 81, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Pentoxide (Ta_2O_5), Barium Strontium Titanate (BST), Strontium Bismuth Tantalate (SBT), Aluminum Oxide (Al_2O_3), Zirconium Oxide (ZrO_2) and Hafnium Oxide (HfO_2).

83. The system of claim 69, wherein said top conducting layer is formed of a material selected from the noble metal group.

84. The system of claim 69, wherein said top conducting layer is formed of a non-oxidizing metal permeable to oxygen.

85. The system of claim 69, wherein said top conducting layer is formed of a conducting metal oxide.

86. The system of claim 69, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO_2), Rhodium Oxide (RhO_2), Chromium Oxide (CrO_2), Molybdenum Oxide (MoO_2), Rhemium Oxide

(ReO_3), Iridium Oxide (IrO_2), Titanium Oxides (TiO_1 or TiO_2), Vanadium Oxides (VO_1 or VO_2), and Niobium Oxides (NbO_1 or NbO_2).

87. The system of claim 86, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), and Platinum Iridium (PtIr).

88. The system of claim 69, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said dielectric layer is a layer of Tantalum Oxide.

89. The system of claim 69, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said dielectric layer is a layer of Barium Strontium Titanate (BST).

90. The system of claim 69, wherein said top conducting layer is formed of a material selected from the group consisting of: Platinum, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said bottom conducting layer is a layer of Tungsten Nitride (WNx, WN, or W_2N) layer and said dielectric layer is a layer of Aluminum Oxide (Al_2O_3).

91. The system of claim 69, wherein said post deposition annealed top conducting layer is annealed with an oxygen compound.

92. The system of claim 91, wherein said oxygen annealed layer is annealed in the presence of a material selected from the group consisting of: Oxygen (O_2), Ozone (O_3), Nitrous

Oxide (N_2O), Nitric Oxide (NO), and a gas mixture containing Oxygen (O_2), Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O).

93. The system of claim 91, wherein said oxygen annealed layer is annealed in the presence of a gas mixture containing at least one element selected from the group consisting of: Oxygen (O_2); Ozone (O_3), Nitrous Oxide (N_2O), Nitric Oxide (NO), and water vapor (H_2O).

94. The system of claim 91, wherein said oxygen annealed layer is a plasma enhanced anneal layer.

95. The system of claim 94, wherein said oxygen containing anneal is a remote plasma enhanced anneal.

96. The system of claim 91, wherein said oxygen containing anneal is an ultraviolet light enhanced anneal.